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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/575,425	04/10/2006	Sebastien Prouet	FR03 0121 US1	3751

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EXAMINER	
POOS, JOHN W	

ART UNIT	PAPER NUMBER
2816	

NOTIFICATION DATE	DELIVERY MODE
10/22/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary	Application No.	Applicant(s)	
	10/575,425	PROUET ET AL.	
	Examiner	Art Unit	
	JOHN W. POOS	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 August 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 3-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 3-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 April 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1,3-4, 7 and 8 are rejected under 35 U.S.C. 102(b) as being anticipated by Toyota et al. (US 5,963,064).

In regard to Claim 1 (as taught in Figure 1):

A transconductance circuit intended to convert a differential input voltage, supplied as two signals on two inputs (Inp, Inn), into a differential output current (Iop, Ion), characterized in that, where each of the two signals of said differential input voltage is supplied to each input through a follower transistor connected to said input by its emitter (Column 9: lines 35-38) and receives said signal on a control electrode (M1 and M2), each of the two inputs of the transconductance is connected to a respective current source (M3 and M4) that is dynamically controlled by the other input of the transconductance (102), said current source being such that the current supplied to each input by said current source eliminates current variations caused by voltage variations of the input voltage signal (the functionality does not distinguish the structure over the prior art)

wherein the transconductance circuit comprises two sides ((Inp, M1, M3, Ion) and (Inn, M2, M4, and Iop)), each side comprising an input (Inp and Inn), an output (Iop and Ion), at least a first transistor (M3 and M4) having a control electrode (M3 and M4 gate) coupled for receiving

a bias voltage (Vcont), a first electrode connected to said output (M3 and M4 drain connected to Ion) and a second electrode connected to said input (M3 connected to Inp through M1), a second transistor (M1 and M2) having a first electrode (M1 and M2 drain) and a control electrode (M1 and M2 gate) coupled in common to said input (connected to Inn and INP) and a second electrode connected to a power supply terminal (M1 and M2 source connected to ground through 4lss), and wherein the first and second transistors (M1 and M3) of the first side are different from the first and second transistors of the second side (M2 and M4).

In regard to Claim 3:

A transconductance circuit as claimed in claim 1, wherein said first and second transistors are of the same size. (Column 5: lines 11-13)

In regard to Claim 4 (as taught in Figure 1):

A transconductance circuit as claimed in claim 1, wherein each side further includes a third transistor (M10) of the same size as said second transistor, said third transistor has a control electrode coupled to said first transistor (M10 gate connected through M10 drain) and control electrodes of said second transistor (M10 gate connected through M10 drain and M1), a first electrode connected to the output of the other side (M10 drain connected through M11 and M13) and a second electrode connected to said power supply terminal (M10 source connected to supply (slashed line connected to M10)).

In regard to Claim 7:

A chip intended to be implemented in a transceiver including at least a transconductance as claimed in claim 1. (Column 9: lines 43-46)

In regard to Claim 8:

A transceiver of radio-frequency signals including at least one chip as claimed in claim 7. (Column 9: lines 44-45)

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Toyota et al. (US 5,963,064) in view of Seevnick et al. (US 4,682,098).

In regard to Claim 5:

All of the claim limitations have been discussed with respect to Claim 1 above, except for wherein said current source includes a current mirror mirroring the current passing through said second transistor with a gain of two.

Seevnick (098) teaches wherein said current source includes a current mirror mirroring the current passing through said second transistor with a gain of two (Column 3: lines 5-7).

Therefore it would have been obvious to one skilled in the art at the time of the invention to use a current mirror with a gain of two in order to provide a voltage-current converter which has a linear voltage-current conversion over a relatively large frequency range (Seevnick Column 1: lines 58-61).

6. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Toyota et al (US 5,963,064) and Seevnick et al. (US 4,682,098) as applied to claim 5 above, and further in view of Hughes (US 4,973,857).

In regard to Claim 6:

All of the claim limitations have been discussed with respect to Claims 1 and 5 above, except for wherein said current mirror includes a mirror transistor of twice the size of said second transistor, said mirror transistor having a control electrode connected to the first and control electrodes of said second transistor, a first electrode connected to the input of the other side and a second electrode connected to said power supply terminal.

Hughes (857) teaches wherein said current mirror includes a mirror transistor of twice the size of said second transistor (Column 2: lines 40-49), said mirror transistor having a control electrode connected to the first and control electrodes of said second transistor, a first electrode connected to the input of the other side and a second electrode connected to said power supply terminal (Figure 2: 32 (i.e. 36-1 and 34)).

Therefore it would have been obvious to one skilled in the art at the time of the invention to use a current mirror that is twice the size of the second transistor in order to avoid errors due to "end-effects" in different-sized transistors (Hughes Column 2: lines 50-52).

Response to Arguments

7. Applicant's arguments filed 5 August 2008 have been fully considered but they are not persuasive.

Applicant's argument is that the first and second transistors of the first side are different from the first and second transistors of the second side. This is not persuasive because the transistors M1 and M3 of the first side are different transistors from the transistors M2 and M4 of the second side.

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Communication

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JOHN W. POOS whose telephone number is (571)270-5077. The examiner can normally be reached on M-F (alternating Fridays off), E.S.T.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lincoln Donovan can be reached on 571-272-1988. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Kenneth B Wells/
Primary Examiner, Art Unit 2816

/J. W. P./
Examiner, Art Unit 2816